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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/091,461	03/07/2002	Masataka Ito	00862.022541	8794

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FITZPATRICK CELLA HARPER & SCINTO
30 ROCKEFELLER PLAZA
NEW YORK, NY 10112

EXAMINER	
ISAAC, STANETTA D	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 06/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/091,461	ITO, MASATAKA	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,10-17,19 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10-17,19 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action in response the election and RCE filed on 5/20/05 and 7/13/04, respectively. Currently, claims 1-8, 10-17, 19 and 20 are pending.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 7/13/04 has been entered.

Election/Restrictions

Claims 6, 7, 15 and 16 are directed to the product by process claims and have been rejoined. Since all claims previously withdrawn from consideration under 37 CFR 1.142 have been rejoined, the restriction requirement made in the Office action mailed on 1/07/05 and 4/22/05, respectively is hereby withdrawn.

Specification

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 10-15, 17 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Ito et al. US Patent 6,407,367.

The applied reference has a common Assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Ito discloses the semiconductor method and device as claimed. See figures 1-13, and corresponding text, where Ito teaches, pertaining to claim 10, an annealing method of annealing an SOI, comprising: holding the SOI substrate **W** in a reducing atmosphere containing hydrogen by a holding portion **4** and annealing the SOI substrate (figure 1; col. 3, lines 40-52; col. 4, lines 9-11), wherein the holding portion contains no silicon carbide formed by sintering and has a surface formed from silicon carbide deposited by CVD (figure 1; col. 4, lines 12-19).

Ito teaches, pertaining to claim 11, wherein the annealing is executed at a temperature lower than a melting point of single-crystal silicon (col. 10, lines 30-52).

Ito teaches, pertaining to claim 12, wherein the annealing is executed at a temperature not less than 775°C (col. 10, lines 30-52).

Ito teaches, pertaining to claim 13, wherein the annealing is executed at a temperature not less than 966°C (col. 10, lines 30-52).

Ito teaches, pertaining to claim 14, wherein the annealing is executed at a temperature not less than 993°C (col. 10, lines 30-52).

Ito teaches, pertaining to claim 15, an SOI substrate manufacturing using an annealing method of claim 10 (col. 10, lines 30-52).

Ito teaches, pertaining to claim 17, a semiconductor device manufacturing method, comprising the steps of: annealing an SOI substrate using an annealing method of claim 10 (col. 10, lines 30-52); and forming an active region for a transistor in a semiconductor layer of the SOI substrate (col. 4, lines 54-67; col. 5, lines 1-5).

Ito teaches, pertaining to claim 20, a semiconductor device manufacturing method, comprising the steps of: preparing an SOI substrate manufactured using an annealing method of claim 10 (col. 10, lines 30-52); and forming an active region for a transistor in a semiconductor layer of the SOI substrate (col. 4, lines 54-67; col. 5, lines 1-5).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ito et al., US Patent 6,407,367.

Ito discloses the semiconductor method and device substantially as claimed. See preceding rejection of claims 10-15, 17 and 20 under 35 U.S.C. 102(e).

However, Ito fails to show, pertaining to claims 7 and 16, wherein an HF defect density is not more than 0.05 defects/cm^3.

Ito teaches, controlling the contamination of the surface of the SOI substrate by using a boat that has pure silicon carbide (col. 2, lines 15-20; col. 5, lines 13-27).

It would have been obvious to one of ordinary skill in the art to incorporate having a HF defect density not more than 0.05 defects/cm^3, in the method of Ito, according to the teachings of Ito, with the motivation that, by controlling the contamination of the SOI substrate the amount of defect would also be decreased, therefore would result in routine experimentation.

Claims 1-8 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zehavi et al., US Patent 6,727,191 in view of Ito et al., US Patent 6,407,367.

Zehavi discloses the semiconductor method and device as claimed. See figures 1-5, and corresponding text, where Zehavi shows, pertaining to claim 1, an annealing method of annealing an substrate, comprising: holding the substrate **30** in a reducing atmosphere containing hydrogen by a holding portion **16, 18, 20, 22** having a surface formed form silicon and annealing

the substrate (figure 1; col. 3, lines 19-43), wherein the holding portion is a member having a silicon film thereon or a member formed from single-crystal silicon or polysilicon (col. 3, lines 20-43). In addition, Zehavi shows, pertaining to claim 2, wherein the annealing is executed at a temperature lower than melting point of single-crystal silicon (col. 4, lines 50-65). Also, Zehavi shows, pertaining to claim 3, wherein the annealing is executed at a temperature not less than 775°C (col. 4, lines 50-60; col. 5, lines 1-5). Zehavi shows, pertaining to claim 4, wherein the annealing is executed at a temperature not less than 966°C (col. 4, lines 50-60; col. 5, lines 1-5). In addition, Zehavi shows, pertaining to claim 5, wherein the annealing is executed at a temperature not less than 990°C (col. 4, lines 50-60; col. 5, lines 1-5). Also, Zehavi shows, pertaining to claim 6, a substrate manufactured using an annealing method of claim 1 (figure 1; col. 3, lines 19-43). Zehavi shows, pertaining to claim 8, a semiconductor device manufacturing method, comprising the steps of: annealing a substrate using an annealing method of claim 1 (figure 1; col. 3, lines 19-43). Finally, Zehavi shows, pertaining to claim 19, a semiconductor device manufacturing method, comprising the steps of: preparing a substrate manufactured using an annealing method of claim 1 (figure 1; col. 3, lines 19-43).

However, Zehavi fails to show, pertaining to claims 1, 6 and 8, an annealing method of annealing an SOI substrate, comprising: holding the SOI substrate. In addition, Zehavi fails to show, pertaining to claim 7, wherein an HF defect density is not more than 0.05 defects/cm^3. Finally, Zehavi fails to show, pertaining to claims 8 and 19, forming an active region for a transistor in a semiconductor layer of the SOI substrate.

Ito teaches, a similar manufacturing method that includes holding an SOI substrate and applying an annealing method that includes a reducing atmosphere containing hydrogen. In

addition, Ito teaches the formation of an active region for a transistor device (col. 4, lines 65-67; 5, lines 1-5; col. 10, lines 30-52).

It would have been obvious to one of ordinary skill in the art to incorporate a method of annealing an SOI substrate, comprising: holding the SOI substrate; forming active region for a transistor in a semiconductor layer of the SOI substrate, in the method of Zehavi, according to the teachings of Ito, with the motivation of performing a more efficient heat treatment without reducing the thickness of the SOI layer on the substrate. In addition, SOI substrates are conventionally well known in the art of transistor manufacturing, where it would be desirable to one of ordinary skill in the art to have an active region formed on an SOI substrate, with the motivation of creating a more efficient semiconductor device, such an increase in circuit speed and a reduction in parasitic capacitance. Finally, based on the combined teachings of Zehavi in view of Ito, having a defect density of not more than 0.05 defects/cm^3 would result in routine experimentation, since ultimately the goal would be the creation of an active region having as little contamination (defect) as possible, especially since no criticality is shown.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stanetta Isaac
Patent Examiner
June 6, 2005

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812